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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/831,241	05/03/2001	Simon Pearce	R&G C-321	4577

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EXAMINER
CASCHERA, ANTONIO A

ART UNIT	PAPER NUMBER
2697	9

DATE MAILED: 06/18/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/831,241	PEARCE, SIMON	
	Examiner	Art Unit	
	Antonio A Caschera	2697	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) *1 and 7* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2-6 and 8-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 May 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *3-6* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 2, 10 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schilling et al. (U.S. Patent 6,236,405 B1) in view of Winser (GB 2,240,016 A).

In reference to claim 2, Schilling et al. and Winser disclose all of the claim limitations as applied to claim 10 in addition, Schilling et al. discloses a compression/decompression means for compressing/decompressing texture data stored in memory (see columns 5-6, lines 45-13).

In reference to claim 10, Schilling et al. discloses a three-dimensional graphics system incorporating a texture mapping methods (see column 2, lines 7-9 and column 4, lines 27-29). Schilling et al. also discloses a memory means for storing mip-map data for use in texturing an image, the mip-map data made up of levels of decreasing resolution (see column 4, lines 9-23 and Figure 2). Schilling et al. discloses a cache, coupled to a DRAM controller, which stores color data, which in the present invention represents the texture data, retrieved from memory (see column 7, lines 37-44 and #614 of Figure 6). Schilling et al. also discloses a color extract unit, connected to the cache, which selects data from four received 64-bit quantities for use by an interpolator according to pixel center coordinates received from the DRAM controller (see column 7, lines 45-49). Note the office interprets such a unit substantially similar in

functionality to the lower-level mip-map generator, coupled to a cache, generating portions of mip-map next below in the hierarchical series of mip-maps which must be in accordance with a pixel centers coordinates. Schilling et al. discloses a bilinear interpolation performed on four neighboring texel colors in accordance with the pixel center coordinates (see column 7, lines 49-55). Schilling et al. discloses the interpolator coupled to receive data from the cache via the color extraction unit and output data to a rasterizer (see #607, 614, 618 and 622 of Figure 6). Schilling et al. also discloses a modified embodiment of the invention where a complete trilinear interpolation is performed instead of a bilinear interpolation (see column 7, lines 56-60). Schilling et al. does not explicitly disclose an input means for receiving input data indicating the type of mip-map data required and the level of the mip-map however Winser does. Winser discloses a display apparatus for real-time three-dimensional image synthesis implementing texture mapping (see page 1, lines 3-20). Winser discloses a texture management circuit (see #49 of Figure 3) which has inputs to receive texture u, v coordinates as well as texture pyramidal level L coordinates from a display processing unit (see page 14, lines 31-32). Winser also discloses control means coupled to the input means and memory means to retrieve a mip-map from memory as Winser discloses a page location and logic circuit (see pages 14-15, lines 32-24 and #50 of Figure 3). Winser also discloses an interpolation means for creating an output texel from two bilinearly interpolated values MOD1 and MOD2 which were derived from different map values of different levels (T.Li and T.Li+1) (see page 20, lines 1-11). It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the input and control means of Winser with the three-dimensional texture mapping system of

Schilling et al. in order to provide efficient access to texture data stored on a medium of a graphics texturing system.

Claim 14 is similar in scope to claim 10 and therefore is rejected under similar rationale.

2. Claims 3-6 and 11-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schilling et al. (U.S. Patent 6,236,405 B1), Winser (GB 2,240,016 A) and further in view of Fowler et al. (U.S. Patent 6,339,428 B1).

In reference to claim 3, Schilling et al. and Winser disclose all of the claim limitations as applied to claim 2 above, however neither Schilling et al. nor Winser explicitly disclose the decompression means coupled to a cache, trilinear interpolator and lower-level mip-map generator. Fowler et al. discloses a decompression block coupled to multiple caches, filtering blocks which performs interpolation calculations and a blending block which combines the outputs of the filtering blocks (see #40, 50, 60, 70, 160 and 180 of Figure 2). It would have been obvious to one of ordinary skill in the art at the time the invention was made to arrange the decompression means coupled to a cache on its input, as disclosed by Fowler et al., in order to receive compressed texture data to decode and a trilinear interpolator and a mip-map generator on its output, as disclosed by Fowler et al., in order to further process and calculate a texture value for certain pixel coordinates by processing texels in close vicinity of the certain pixel.

In reference to claim 4, Schilling et al. and Winser disclose all of the claim limitations as applied to claim 2 above. Neither Schilling et al. nor Winser explicitly disclose cache means coupled to decompression means arranged in parallel however Fowler et al. does. Fowler et al. discloses a method and apparatus for reducing memory bandwidth in a graphics texturing system (see lines 1-2 of abstract). Fowler et al. discloses the apparatus to include multiple caches

coupled to decompression blocks (four per block #52, 54, 56, 58 and #162, 164, 166 and 168 all of Figure 2) arranged in parallel (see #40, 50 and 160 of Figure 2). Fowler does not explicitly disclose 4 caches however Fowler et al. does disclose including additional caches to facilitate handling even more texture information in the graphics system (see column 6, lines 2-5). Further, the office interprets the particular design using 4 separate caches to be a matter of design choice as preferred by the designer of the graphics system as a single cache could be used instead of four separate caches as long as the single cache has enough read/write ports and sufficient storage to handle the texturing system's demands (see column 6, lines 9-12 of Fowler et al.). It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the input and control means of Winser and the three-dimensional texture mapping system of Schilling et al. with the texture cache/decompression configuration of Fowler et al. in order to reduce memory bandwidth in a texturing system by utilizing local texture caches storing less data in a compressed form (see column 2, lines 25-42 of Fowler et al.).

In reference to claim 5, Schilling et al. and Winser disclose all of the claim limitations as applied to claim 2 above. Neither Schilling et al. nor Winser explicitly disclose an allocating means for allocating the outputs of different caches to selected ones of the decompression means however Fowler et al. does. Fowler et al. discloses, "...a texture address module which provides control information to the plurality of caches such that texture data for texturing operations is provided at the outputs of one or more of the plurality of caches," (see column 6, lines 49-53 and #30 of Figure 2). The office interprets the texture address module to be substantially similar in functionality to the allocating means found in applicant's claim. Fowler et al. does not explicitly disclose the location of such an address module between the cache and decompression units

however the office sees this limitation as a matter of design choice as preferred by the designer as the exact location of the texture address module is not critical as long as the module is coupled to and controls the output data from the caches (see column 6, lines 52-53 of Fowler et al.). It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the input and control means of Winser and the three-dimensional texture mapping system of Schilling et al. with the texture cache/decompression configuration, including the texture address module of Fowler et al., in order to distribute data from a plurality of storage units to a plurality of processing units efficiently maximizing processing output.

In reference to claim 6, Schilling et al. and Winser disclose all of the claim limitations as applied to claim 10 above. Neither Schilling et al. nor Winser explicitly disclose the lower-level mip-map generator comprising four interpolators which operate on 16 texels from the mip-map held in the cache to provide four texels however Fowler et al. does. Fowler et al. discloses the apparatus to include multiple caches coupled to decompression blocks (four per block #52, 54, 56, 58 and #162, 164, 166 and 168 all of Figure 2) arranged in parallel (see #40, 50 and 160 of Figure 2). Fowler does not explicitly disclose four caches however Fowler et al. does disclose including additional caches to facilitate handling even more texture information in the graphics system (see column 6, lines 2-5). Further, the office interprets the particular design using four separate caches to be a matter of design choice as preferred by the designer of the graphics system as a single cache could be used instead of four separate caches as long as the single cache has enough read/write ports and sufficient storage (see column 6, lines 9-12 of Fowler et al.). Fowler et al. also discloses filtering units coupled to the output of decompression units used to, "...filter uncompressed texture data provided by the decompression blocks," (see column 7, lines

9-10 and #60 and 180 of Figure 2). Fowler et al. also discloses the filtering block to comprise, for example, of bilinear filtering operations which receive four texels each and output one resultant texture color each (see column 7, lines 11-12). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to expand the amount of caches, decompression and filtering units to 4, thus operating on 16 texels, with the input and control means of Winser and the three-dimensional texture mapping system of Schilling et al. in order to facilitate the handling of more texture information in the graphics texturing system (see column 6, lines 2-5 of Fowler et al.).

In reference to claim 11, Schilling et al. and Winser disclose all of the claim limitations as applied to claim 4 above. Claim 11 is similar in scope to claim 5 and therefore is rejected under similar rationale.

In reference to claim 12, Schilling et al. and Winser disclose all of the claim limitations as applied to claim 4 above. Claim 12 is similar in scope to claim 6 and therefore is rejected under similar rationale.

In reference to claim 13, Schilling et al. and Winser disclose all of the claim limitations as applied to claim 5 above. Claim 13 is similar in scope to claim 6 and therefore is rejected under similar rationale.

3. Claims 8 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fowler et al. (U.S. Patent 6,339,428 B1).

In reference to claims 8 and 9, Fowler et al. discloses a compression technique utilized to compress individual texels in a graphics texturing system comprising of two 16-bit color values which are used as reference colors for each texel block (see column 3, lines 51-57). Fowler et al.

also discloses each of the texels in a 4x4 block being represented by a 2-bit encoding where the encoding selects one of the two 16-bit colors, a combination of two colors or a transparent color for the texel (see column 3, lines 57-61). Fowler et al. discloses an example of such an encoding technique where a first reference color is chosen to be blue and a second as red from which two shades of purple are created where certain proportions of red and blue contribute towards the final shade (see columns 3-4, lines 62-8). Fowler et al. also discloses interpolating a resultant texel from input texels using the compressed color coded values which are retrieved from cache, uncompressed and then processed (see column 7, lines 10-14). Fowler et al. does not explicitly disclose defining other coded colors from weighted averages of principal colors however it would have been obvious to one of ordinary skill in the art at the time the invention was made to implement calculation means using weighted averages of principal colors to create secondary colors as such a technique is well known in the graphics processing art and is commonly practiced. Further, it is well known in the art that secondary colors are created from mixing varying amounts of primary colors therefore calculating weighted averages of color codes to create other colors would have been obvious to one of ordinary skill in the art at the time the invention was made.

References Cited

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

a. Wood (U.S. Patent 6,295,070 B1)

- Wood discloses an image texture mapping system in a 3-D graphics system where texture maps are stored at different resolutions in a pyramidal array.

b. Munshi et al. (U.S. Patent 6,469,700 B1)

- Munshi et al. discloses per pixel mip mapping and trilinear filtering where the performance of the trilinear filtering is improved by reducing the number of computations performed.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Antonio Caschera whose telephone number is (703) 305-1391. The examiner can normally be reached Monday-Thursday and alternate Fridays between 7:00 AM and 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Joseph Mancuso, can be reached at (703)-305-3885.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 872-9314 (for Technology Center 2600 only)

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

aac

5/19/03

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